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MULTI-MODE EXCITING FOR STEPPING MOTOR

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Abstract. *This paper presents a method for generating, grouping, and classifying exciting signals of stepping motor in three modes. Moreover, the method can combine all modes together to obtain the wide speed response. The proposed method decodes each exciting signal to digital pulse and arranges as 1-bit output in ROM. The research generates 12 exciting signals and classifies into 3 groups for 3-mode exciting; full step, half step and sinusoidal mini step. Each mode can be selected by manual or automatic that depends on how speed responds and torque demands. In addition, the automatic selection is designed to improve motor speed in wide range. All digital circuits and ROM are constructed using Field Programmable Gate Array (FPGA) and Verilog Hardware Description Language (Verilog HDL) so that the proposed technique has small size and can be easily to be implemented. The speed responses are studied using a 4-phase Permanent Magnet Stepping Motor (PMSM) as an illustrative case study. The experimental results show that speed responses of each mode and combined mode are in agreement with the theoretical values.*
Keywords: Exciting signal, Full step, Half step, Mini step, Stepping motor, FPGA

1. **Introduction.** A stepping motor can be excited by several signals, which are dependent on movement functions and loads. The full step exciting is the simplest drive that excites either two-phase-on or one-phase-on, it develops the high torque as well as the good braking, but the step movement is coarse [1]. The half step exciting is a method to subdivide from one step to half step. This exciting has the continuous torque and the high speed response. The sinusoidal mini step exciting subdivides each step into mini step for stepless, high speed response, and continuous torque [2]. This research concerns with 3-mode exciting and decoding signals to binary data before saving in ROM. The 1-bit multi-channel technique [3] is used to arrange the data and group into multi-mode exciting. In addition, all modes can combine together to achieve the wide speed response. All of the components used in the proposed system are implemented using FPGA and Verilog HDL [4], so that the propose technique has the advantages of simple implementation and better capability of application.

2. **Principle and Theory of Stepping Motor.** A basic 4-phase PMSM consists of a rotating permanent magnet surrounded by 4 stator poles. Its cross section can be shown in the Figure 1.

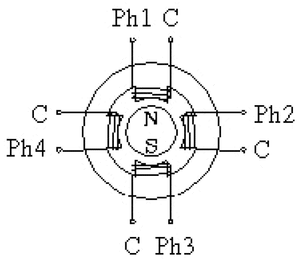

FIGURE 1. Cross section of the 4-phase PMSM

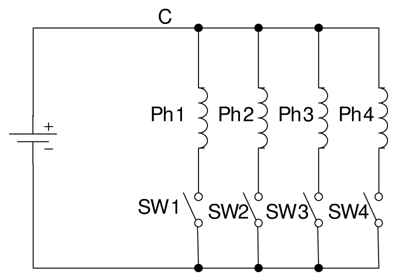

FIGURE 2. Schematic of the excitation of 4-phase PMSM

2.1. **Excitation of the 4-phase PMSM.** Figure 2 shows the schematic of the excitation of 4-phase PMSM. The terminal C is a common of stator winding that is connected to the positive polarity of power supply. If each phase is excited in sequence Ph1, Ph2, Ph3, and Ph4, respectively. The stepping motor will be driven in clockwise and the step angle is 90 $^{\circ}$. For the rotation of PMSM, the speed and direction are dependent on the frequency and the pulse sequence of exciting signals, respectively.

2.2. **Full step mode.** Full step mode can excite either "one-phase on" or "two- phase on". For one-phase on, only one phase is excited for each step. Otherwise, the two-phase on, both phases are excited together for each step. This mode provides the highest torque. Their exciting signals can be shown in the Figure 3 and Figure 4, respectively.

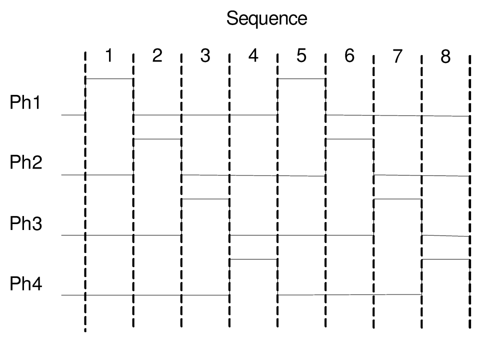

FIGURE 3. Exciting signals for one-phase on full step mode

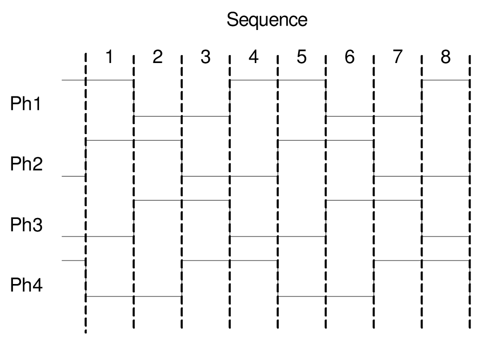

FIGURE 4. Exciting signals for two-phase on full step mode

2.3. **Half step mode.** This mode is excited alternately between one-phase on and two-phase on, so that the motor moves in half step increments. This sequence halves the effective step angle of the motor, but it gives the less regular torque. The exciting signals can be shown in the Figure 5.

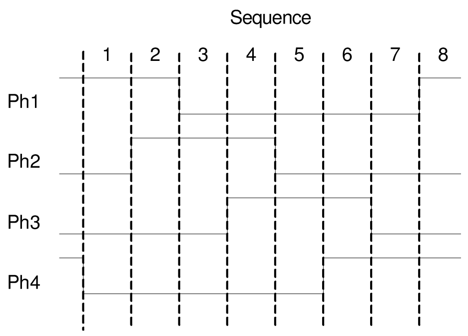

FIGURE 5. Exciting signals for half step mode

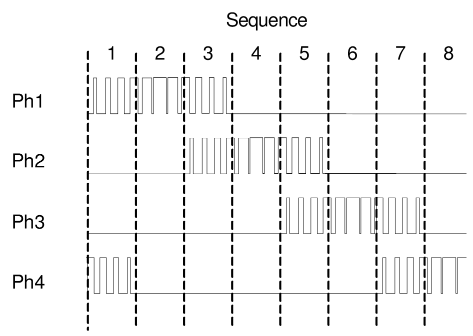

FIGURE 6. Exciting signals for sinusoidal mini step mode

2.4. **Sinusoidal mini step mode.** In sinusoidal mini step or micro step drive, the natural step is subdivided into many small steps as sinusoidal pulse width modulation (SPWM), which can be shown in the Figure 6. This mode uses SPWM signal for exciting instead of pulse signal.

3. **Design of Multi-mode Exciting.** The driver of the proposed system uses 4 switches. Each switch is IRF 520N to drive each phase of the 4-phase PMSM. The hardware implementation is based on FPGA model Acex1K50-144-3. Block diagram of the proposed technique can be shown in the Figure 7, which consists of counter, ROM, and output selector. The counter is an 8-bit counter which is designed to count up or down between 0-167. The ROM saves the binary data of exciting signals which are classified to 3 modes.

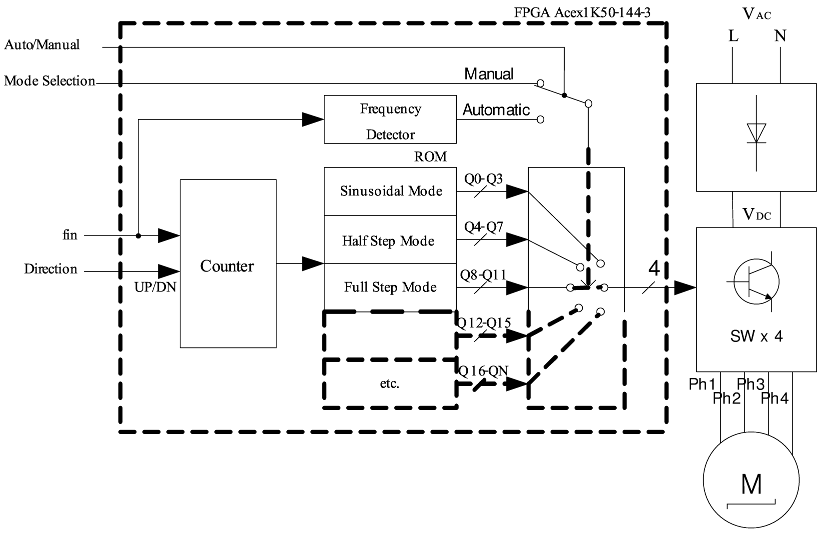

FIGURE 7. Block diagram of multi-mode exciting

The outputs of sinusoidal mode, $Q_0 - Q_3$, are the SPWM signals. The concept of each SPWM segment can be shown in Figure 8 and Figure 9, respectively.

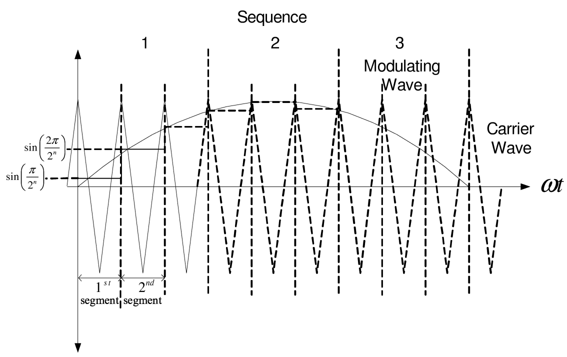

FIGURE 8. Concept of SPWM

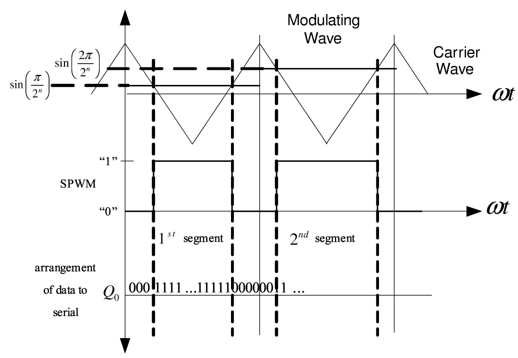

FIGURE 9. Each segment of SPWM

Each segment is decoded to binary data, which have the resolution of 2^7. The logic state of each segment depends on the comparison between carrier wave (saw tooth signal) and the amplitude of modulating wave (sinusoidal signal). All exciting signals are arranged as 1-bit serial data and saved in ROM. Its output data are grouped and classified into 3 modes, which are sinusoidal mini step, half step, and full step mode. The arrangement of data and their outputs can be shown in Figure 10.

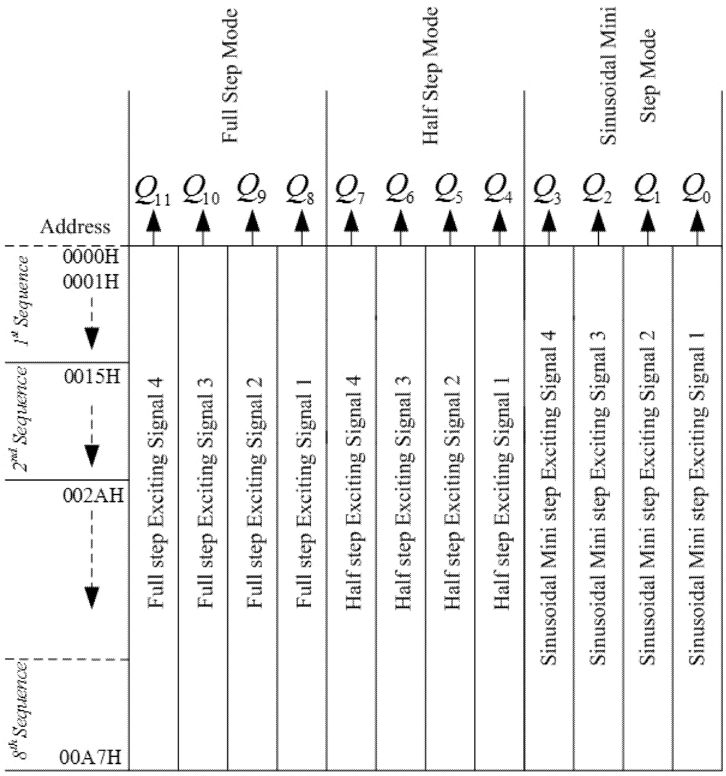

FIGURE 10. Arrangement of exciting signals in ROM

Serial data in ROM are arranged into 12-bit output signals, which are grouped into 3-mode exciting, where

$Q_0 - Q_3$ are the output signals for sinusoidal mini step mode.

$Q_4 - Q_7$ are the output signals for half step mode.

$Q_8 - Q_{11}$ are the output signals for full step mode.

All modes have the data for 8 sequences of exciting signal. When read data from ROM, all bits are fed to its output whereas only one mode is selected to driver at the same time.

4. **Experimental Results.** The system was implemented by Verilog HDL and FPGA model EP1K50TC144. Its capacity is 50,000 gates and output voltage is 3.3 volts [5]. The output signals were measured by 4-channel isolated oscilloscope. Tektronix AFG3021 arbitrary/function generator is used as input clock.

4.1. **Exciting signal testing.** Input clock fin was set to 10kHz and fed to 167 counter for decoding exciting signals. The four channels (CH1-CH4) of oscilloscope are used to show that experimental results of each mode exciting signals. Figure 11 - Figure 13 show the experimental results of full step, half step, and sinusoidal mini step mode, respectively.

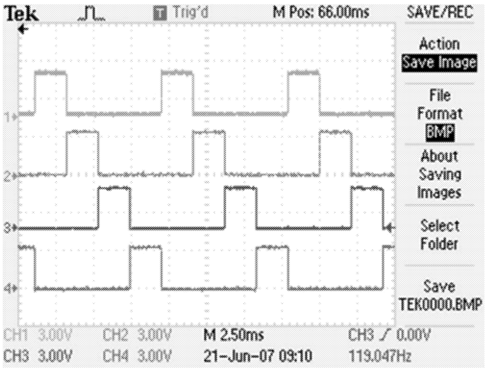

FIGURE 11. Full step mode

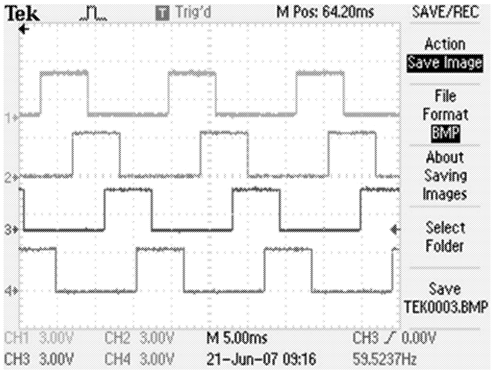

FIGURE 12. Half step mode

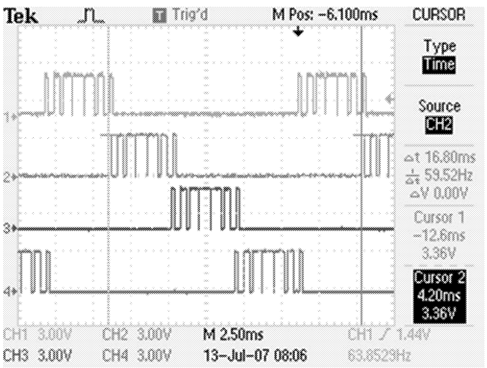

FIGURE 13. Sinusoidal Mini step mode

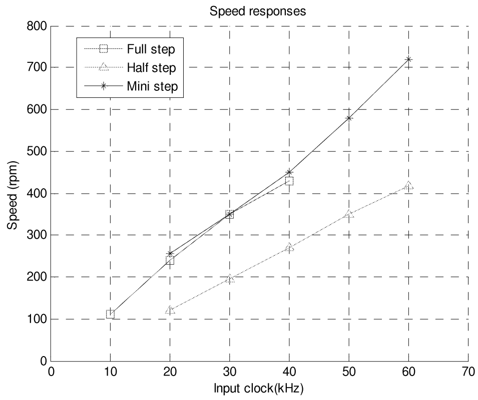

FIGURE 14. Speed responses and input clock of each mode

4.2. **Speed responses.** In order to test speed responses of the proposed technique, the input clock fin was adjusted. The stepping motor is the 4-phase PMSM, which has resolution 1.8 degree per step and the resistance is equal to 0.8Ω per phase. The experimental results in Figure 14 show the speed responses of each mode by manual selection, where the square shape, triangle shape, and star shape show the speed responses of full step mode, half step mode, and sinusoidal mini step mode, respectively. The input clock starts at 10kHz, the full step mode can be excited and the speed response is equal to 100rpm, but other modes are not response. The maximum frequency of full step mode is 40kHz at 420rpm. The half step mode can be excited by the higher frequency of input clock, so the speed response is higher than full step mode. Similarly, the sinusoidal mini step mode provides the highest speed response for input clock from 20kHz to 60kHz. Moreover, this mode can design for the higher speed response by higher resolution exciting signals. Figure 15 shows the speed response which rearranges the exciting data of half step mode and combines 3 modes together to obtain the wide speed responses.

5. **Conclusions.** The proposed system was implemented using FPGA, so that the hardware has small size and ease of implementation. The technique to provide exciting signals for the stepping motor has been described in this paper. These exciting signals are decoded and arranged in 1-bit serial data, and then the use of ROM is much less. The driving function can be easily selected from manual or automatic according to user's

requirement. The experimental results show that the full step exciting mode has good performance at low speed. While the half step and sinusoidal mini step exciting have good speed responses at higher frequency and smooth rotating. Moreover, the technique can combine 3 modes together to achieve the wide speed response.

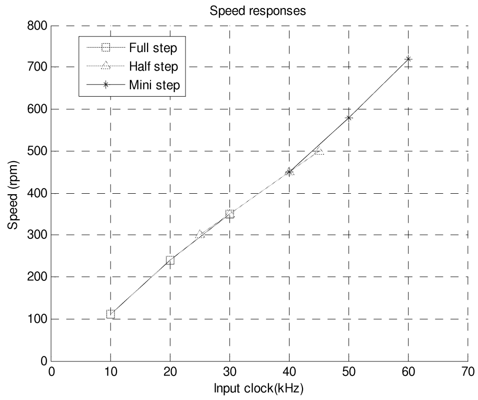

Figure 15. Speed responses when combines 3 modes together

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